IN THE CLAIMS:

This listing of the claims replaces all prior versions and listings of the claims in this application.

The text of all pending claims (including any withdrawn claims) is set forth below. Canceled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (Original), (Currently amended), (Canceled), (Withdrawn), (Previously presented), (New), and (Not entered).

No claims have been amended.

1.–11. (Canceled)

12. (Previously presented) A thin film transistor (TFT), comprising:

a substrate;

a semiconductor layer formed over said substrate having end portions;

a first insulating layer disposed on said semiconductor layer so as to expose end portions of said semiconductor layer;

a gate electrode formed over said first insulating layer;

a capping layer formed over said gate electrode;

spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer;

high-density source and drain regions formed at the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions being spaced apart from the gate electrode and the capping layer;

low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions under said spacers; and

source and drain electrodes which respectively contact said high-density source and drain regions without contact holes.

13. (Canceled)

14. (Original) The TFT of claim 12, wherein said first insulating layer, said capping layer and said spacer are one of an oxide layer and a nitride layer.

15. (Previously presented) The TFT of claim 12, further comprising a silicide layer formed between said source electrode and said high-density source region and a silicide layer formed between said drain electrode and said high-density drain region.

16. (Previously presented) The TFT of claim 15, wherein said silicide layers comprise a refractory metal.

17.–21. (Canceled)

22. (Previously presented) An active matrix display device, comprising:

a substrate;

a semiconductor layer having end portions formed over said substrate;

a first insulating layer formed over said semiconductor layer so as to expose end portions of said semiconductor layer;

a gate electrode formed over said first insulating layer;

a capping layer formed over said gate electrode;

spacers formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer;

high-density source and drain regions formed at entireties of the end portions of said semiconductor layer exposed beyond said spacers;

low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at entireties of off-set regions of said semiconductor layer entirely under said spacers, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers;

source and drain electrodes which respectively contact said high-density source and drain regions without contact holes;

a planarization layer having an opening portion which exposes a portion of one of said source and drain electrodes; and

a pixel electrode formed on the planarization layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion.

23. (Canceled)

24. (Previously presented) The active matrix display device of claim 22, further comprising a silicide layer formed between said source electrode and said high-density source region and a silicide layer formed between said drain electrode and said high-density drain region.

25. (Original) The active matrix display device of claim 22, further comprising an organic electro-luminescence (EL) layer and a cathode electrode sequentially formed on a first predetermined area of said pixel electrode and on a second predetermined area of said planarization layer.

26. (Previously presented) The TFT of claim 12, wherein said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer.

27. (Previously presented) The active matrix display device of claim 22, wherein said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer.

28. (Previously presented) The TFT of claim 12, wherein said high-density source and drain regions are formed at entireties of the end portions of said semiconductor layer exposed beyond said spacers; and

wherein said low-density source and drain regions having a same conductivity as said high-density source and drain regions are formed at entireties of regions of said semiconductor layer entirely under said spacers between the gate electrode and the high-density source and

drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers.